ABSTRACT OF THE DISCLOSURE

In order to test the memory access signal connections between a data processing circuit, such as a processor core 2, and a memory 4, a subset of memory access signal connections 8 are provided with associated scan chain cells 10 so that they may be directly tested. The remainder memory access signal connections 12 which are common to all the expected configurations of the memory 4 are tested by being driven by the processor core 2 itself with data being passed through the memory and captured back within the processor core 2 for checking.

[Figure 2]